K7

Notice of Allowability	Application No.	Applicant(s)	
	10/606,836	AKIYAMA, NAOTO	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the 10-08-04 Amendment*.

2. ☒ The allowed claim(s) is/are *1,3 and 5-10*.

3. ☒ The drawings filed on *08 October 2004* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20041222*.
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Shouxiang Hu

SHOUXIANG HU
PRIMARY EXAMINER

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with David A. Blumenthal (RN: 26,257) on December 20, 2004.

The application has been amended as follows:

IN THE TITLE

The title is changed to: --A semiconductor Device Having a Protection Circuit--.

IN THE CLAIMS

1. (Currently amended) A semiconductor device comprising:

a substrate; and

a plurality of groups of transistors formed on said substrate to be operated by a common voltage generated by a power source, ~~at least some~~ each group of said plurality of groups of transistors having a gate dielectric layer ~~of different~~ differing in thickness from that of the other groups of said plurality of groups of transistors,

wherein one group in ~~of~~ said plurality of groups of transistors having a ~~minimum thickness~~ thinnest gate dielectric layer; one transistor in said one group is selected to serve as a power source protection element, ~~and~~

wherein said one transistor selected as the power source protection element has a higher threshold voltage ~~among any~~ than the other transistors in said one group, and ~~having said minimum thickness gate dielectric layer.~~

wherein said one transistor selected as the power source protection element has a diode type connection.

2. (Cancelled)

3. (Currently amended) The semiconductor device as set forth in Claim 1, wherein said plurality of groups of transistors ~~have two or more gate dielectric layers each having a different film thickness, and said plurality of transistors~~ include at least three types of transistors each having different combinations of thickness of the gate dielectric layer and threshold voltage from each other.

4. (Cancelled)

5. (Currently amended) The semiconductor device as set forth in Claim 1, wherein said plurality of groups of transistors are disposed in an internal circuit surrounded by an I/O interface region.

6. (Currently amended) The semiconductor device as set forth in Claim 1, wherein said plurality of groups of transistors include a high speed processing type transistor and a low power consumption type transistor, and said transistor selected to serve as the power source protection element has a higher threshold voltage than that of said high speed processing type transistor.

7. (Currently amended) The semiconductor device as set forth in Claim 1, wherein said plurality of groups of transistors include a high speed processing type transistor and a low power consumption type transistor, and said transistor selected to serve as the power source protection element has a gate dielectric layer thickness which is the same as or thinner than that of said high speed processing type transistor.

8. (Currently Amended) The semiconductor device as set forth in Claim 1, wherein said plurality of groups of transistors include a high speed processing type transistor and a low power consumption type transistor, and leak current of said transistor selected to serve as the power source protection element is smaller than that of said high speed processing type transistor.

9. (Currently amended) The semiconductor device as set forth in Claim 1, wherein said plurality of groups of transistors include a high speed processing type transistor and a low power consumption type transistor, and said transistor selected to serve as the power source protection element has a higher threshold voltage than that

of said high speed processing type transistor, and said transistor selected to serve as the power source protection element has a gate dielectric layer thickness which is the same as or thinner than that of said high speed processing type transistor.

10. (Currently amended) The semiconductor device as set forth in Claim 9, wherein said plurality of groups of transistors are disposed in an internal circuit surrounded by an I/O interface region.

11-18. (Cancelled).

Allowable Subject Matter

Claims 1, 3, and 5-10 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shouxiang Hu

December 22, 2004 

SHOUXIANG HU
PRIMARY EXAMINER